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Advanced Fault Isolation and Failure Analysis Techniques for Future Package Technologies

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Advanced Fault Isolation and Failure Analysis Techniques for Future Package Technologies

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ABSTRACT

As next-generation package technologies become more complex, the isolation of defects and their failure analysis has became more challenging. The complexity of new-generation packages, driven by Moore's Law, include a greater number of components allocated to smaller form factors, thus creating defects that are difficult to isolate and characterize, such as metal migration, dendrite growth, microcracks, wirebond microfractures, plane-to-plane shorting, high-resistance, defects in multistacked dice, via delamination, and bump bridging. A continued effort has been made to close these technical gaps in analytical tools and techniques. By guiding and co-developing next-generation analytical tools, we have been able to successfully identify failure modes and root causes to rapidly advance unique and new solutions at Intel in current package technologies. In this paper we discuss how these tools are being used in the failure analysis flow, as well as the technical gaps that have to be addressed in order to meet the fault isolation and failure analysis challenges of next-generation package technologies.

INTRODUCTION

The assembly package development roadmap has been increasing the electrical, geometrical, thermal, and material composition complexity of new package technologies, while at the same time reducing the dimensions. As a result of these trends, the isolation and root cause analysis of defects has become increasingly challenging for traditional analytical tools and techniques. In addition, reduced time-to-information and non-destructive approaches have become critical factors, introducing more challenges into the analytical tools development roadmap.

In order to close technical gaps in analytical tools and techniques used in fault isolation and failure analysis, Intel has partnered with suppliers and industry consortia to guide the analytical tool development roadmap. In this paper, we describe some of the key advanced analytical tools and techniques that Intel has co-developed with external metrology companies in the past few years. We divide the paper into three major sections: an overall review of analytical tools and techniques, detailed operation principles and select applications of co-developed tools and techniques, and the challenges of the analytical tool roadmap.

ADVANCED FAULT ISOLATION AND FAILURE ANALYSIS TOOLS

The main body of this paper describes the operation principles and main applications of key advanced analytical tools and techniques that are used at Intel for performing fault isolation and failure analysis. Magnetic fields, acoustics waves, X-ray and thermal radiations, and electric pulses are some examples of input and/or output signals that are used to characterize defects in IC packages.

For failure modes that are electric in nature, such as shorting and high-resistance, next-generation magnetic and current imaging tools have been developed with the capability to non-destructively isolate defects to within a 10-30-micron resolution. This capability is becoming more and more critical as circuit design complexity increases with reduced form factor packages. In cases where the electric failure mode is dead open, current time domain reflectometry can resolve ~200 microns. When the defects produce thermal failure modes like delamination in thermal interface materials, infrared imaging technology has shown excellent results. The use of ultrasound for non-destructive fault isolation and characterization of defects is one of the most applied technologies in the silicon package interaction area. It is the only non-destructive method that can capture mechanical-integrity-related defects or delamination when weaker low-k interlayer dielectric materials are used in silicon. Once the defects have been isolated, a new X-ray computed tomography technology can completely non-destructively characterize the defects by virtual cross sectioning, and in many cases with significantly reduced throughput time. In cases requiring further physical failure analysis, laser deprocessing allows access into the area of interest with greatly reduced probability of damaging the defects, a huge benefit over traditional deprocessing. In order to assess material interfacial strength, a laser spallation technique has been developed and used to study different material stack-ups. Laser spallation techniques have been applied to assembly technology development, such as interlayer dielectric integrity, bump limiting metallurgy integrity, underfill adhesion, copper-to-dielectric, and silicon-to-die attach adhesion.

In this section, we provide a detailed description of the operation principle as well as key applications of these advanced analytical tools and techniques.

Advanced Magnetic Current Imaging Techniques and Applications

The ability to sense very small magnetic fields generated by energized conductive structures makes Magnetic Current Imaging techniques ideally suited for non-destructive detection of circuit defects in buried layers of packages and flip-chip mounted dies from both the front and backside of the unit. One of the most sensitive sensors used for magnetic imaging is the Superconductive Quantum Interference Device (SQUID). When this sensor is used in scanning mode, it can provide a complete map of the magnetic fields generated in an electronic package, and in this case the technique is known as Scanning SQUID Microscopy (SSM). Magnetic microscopy, and in particular SSM, has proved to be a powerful analytical tool in easing the isolation of defects that have an electrical fingerprint, in a non-destructive fashion at relatively large distances from the defect location [1].

In some cases, when the geometrical characteristics of the Device Under Test (DUT) don't allow the SQUID sensor to scan within an appropriate distance from the defect location, a sample preparation may be required (for instance, removing components from the top side of the package or thinning the die). Analyzing electric structures of the failing unit is very important in these cases to ensure that the sample preparation won't damage the defect.

In a typical SSM configuration, a SQUID sensor measures the weak magnetic fields produced by any energized conductive structure of the IC package circuitry. The DUT is moved under the SQUID sensor using motorized micropositioning stages, thus giving a complete map of magnetic information associated with every in-plane scanning data point. A lock-in amplifier filters the alternating magnetic signal produced by the energized circuit structures. Finally, the complete internal electric current image is calculated via the Biot-Savart Law. Figure 1 shows a typical SSM configuration. Experimental data reported in this section were obtained using the SSM Magma-C20.

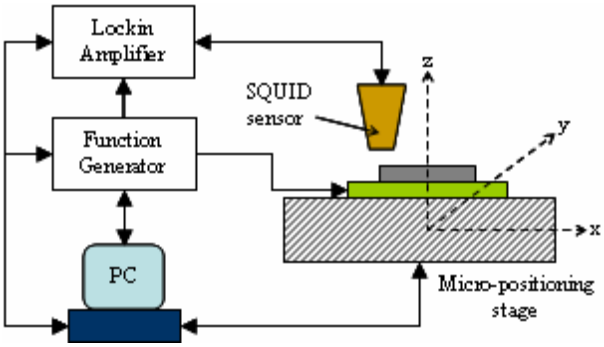


Figure 1: Typical scanning SQUID microscope configuration

The main application of SSM is the isolation of defects that have an electric shorting fingerprint, for instance, metal migration, dendrite growth, wirebond shorts, and bump-to-bump shorts. In order to isolate the short location of two independent circuit structures, the fault isolation procedure consists of energizing the shorted structures, and then comparing the measured current density image with respect to the actual electric circuitry to identify where the energized structures can potentially make the electric connection. This procedure is described in detail in our case studies.

Electric shorts in multi-stacked die packages can be very difficult to isolate non-destructively, especially when a

large number of wirebonds are somehow shorted. For instance, when an electric short is produced by two bond wires touching each other, X-ray analysis may help to identify potential defect locations; however, defects like metal migration produced at wirebond pads, bond wires somehow touching any other conductive structures, or defects that have dimensions smaller than 3-5 microns may be very difficult to identify with non-destructive techniques that are not electrical in nature. Here, the availability of analytical tools that can map out the flow of electrical current inside the package provide valuable information to guide the failure analyst to potential defect locations.

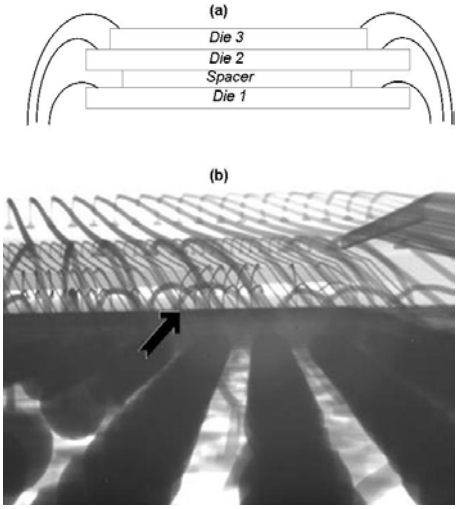


Figure 2: (a) Schematic showing typical bond wires in a triple-stacked die package; (b) X-ray lateral view of actual triple-stacked die package.

Figure 2a shows the schematic of our first case study consisting of a triple-stacked die package. The X-ray image of Figure 2b is intended to illustrate the challenge that finding the potential short locations represented for failure analysts. In particular, this is one of a set of units that were inconsistently failing and recovering under reliability tests. Time domain reflectometry and X-ray analysis were performed on these units but the defects could not be isolated. Also there was no clear indication of defects that could potentially produce the observed electrical short failure mode. Two of those units were analyzed with SSM.

Electrically connecting the failing pin to ground pin produced the electrical current path shown in Figure 3. This electrical path strongly suggests that the current is somehow flowing through all the ground nets through a conductive path located very close to the wirebond pads from the top down view of the package. Based on electrical and layout analysis of the package, it can be inferred that current is either flowing through the wirebond pads or that the wirebonds are somehow touching a conductive structure at the specified location.

After obtaining similar SSM results on the two DUTs, further destructive analysis focused on the small potential short region, and it showed that the failing pin wirebond is touching the bottom of one of the stacked dies at the specific XY position highlighted by SSM analysis.

Another application of the SSM technique is in isolating defects that have a high-resistance failure mode. In this case, the fault isolation procedure consists of performing a magnetic field differential analysis on failing and passing units, which highlights the otherwise negligible alteration in the magnetic field in the failing unit produced by the defect.

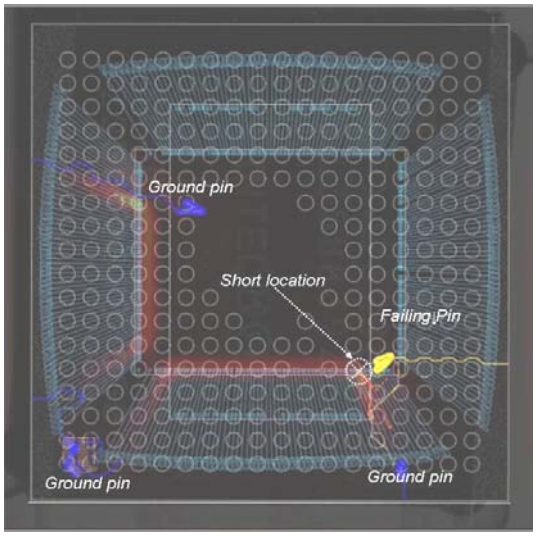


Figure 3: Overlay of current density, optical, and CAD images in triple-stacked die package with electric short failure mode

If electrical shorts in multi-stacked packages represent a challenging case for the failure analyst when SSM was not available, the electrical failures produced by microcracks and/or pad-lifts in wirebonds are definitely more difficult. In these cases, the failure mode is not an electric short, but high resistance. In this case, the information provided by Time Domain Reflectometry (TDR) and X-ray analysis does not usually help in locating the defect due to a fundamental resolution limitation. Again, mapping out what the current is doing inside the package is a powerful piece of information to find potential defect locations, and then further non-destructive and destructive analysis focused on the small highlighted regions usually leads to the defect location.

Figure 4 shows the overlay of the optical image, the CAD layout, and the magnetic-differential image of a dual-stacked die package. In this case, the magnetic differential image was obtained by subtracting the magnetic fields

obtained from failing and passing units. This magnetic differential analysis is necessary because the current density in the failing unit is very similar to the current density of the good one, thus making it very difficult to identify any potential difference between failing and bad units by analyzing current paths only. In other words, the current in both failing and good units follows exactly the same path, and thus they look like exact copies of each other for all practical purposes. Blue and red colors in the magnetic image represent opposite magnetic phase directions. As can be seen, very close to the wirebonds pads there is a clear dipole (red/blue lobe), which is the magnetic field difference between good and failing units due to small current density changes at the defect site, and this is one of the typical signatures of high-resistance defects.

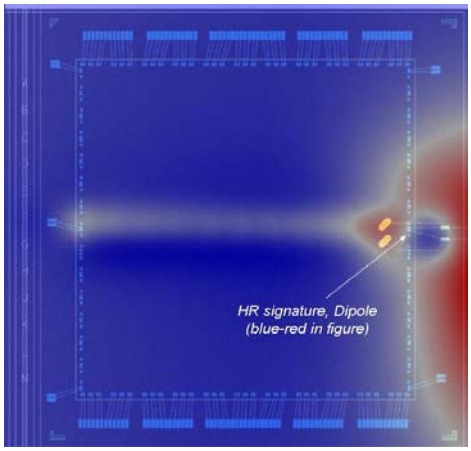


Figure 4: Overlay of magnetic-differential, optical, and CAD images in dual-stacked die package with high-resistance failure mode

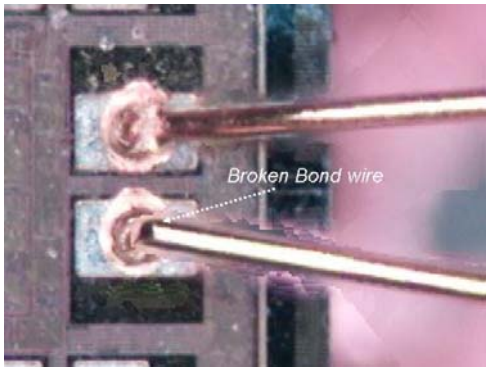


Figure 5: Physical analysis confirming the location of defect in the region highlighted by SSM analysis

The unit was chemically decapsulated to access the wirebond pad region. As shown in Figure 5, the wirebond is broken very close to the pad area that was located with SSM analysis.

Advanced Time Domain Reflectometry Techniques and Applications

TDR is a method for measuring impedance as a function of time of a conductive trace or circuit. With these measurements, fundamental information about a circuit trace can be collected in detail. Typically, a TDR system includes a high-bandwidth digital sampling oscilloscope and a sampling head as shown in Figure 6.

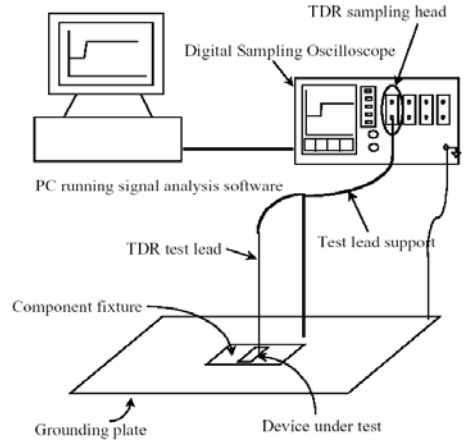


Figure 6: Schematic of TDR system

The TDR sampling head generates a low amplitude pulse, and the oscilloscope measures the reflections from the circuit trace being tested. From these reflections, impedance information can be gathered as a function of time. Whenever energy transmitted through any medium encounters a change in impedance, some of the energy is reflected back toward the source. The amount of energy reflected is a function of the incident energy. The magnitude of the impedance difference and the reflection coefficient can be described in equation (1),

$$\rho = \frac{V_{refect}}{V_{incident}} = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (1)$$

where $V_{reflect}$ and $V_{incident}$ are reflection and incident pulse amplitude, respectively, and Z_L and Z_0 are load impedance and characteristic transmission line impedance. As the defect in the circuit trace, such as a crack, will cause a change in the impedance and thus an amplitude change in the reflection of the propagated signal, one can compare the reflected waveform with that of a golden unit to isolate the fault very effectively. Figure 7 shows a schematic of how TDR can be used to detect opens (high resistance) and shorts.

Figure 8 shows an example of how TDR can help isolate a via delamination failure issue in a package, where the waveform from an actual fail was compared with those of two passing units that terminated at two specific locations, 1C and 2C. The open waveform laid in between 1C and

2C suggests that the open is located between 1C and 2C; a physical cross-section between 1C and 2C confirmed a via delamination in the package.

However, due to rising time delay and signal noise ratio issues seen in a typical TDR, the fault isolation resolution is limited to 200um to 1mm, which is not sufficient for advanced package technologies, as electronic packages are continuously shrinking line spacing and pitches. Advanced TDR development is required to improve the fault isolation resolution.

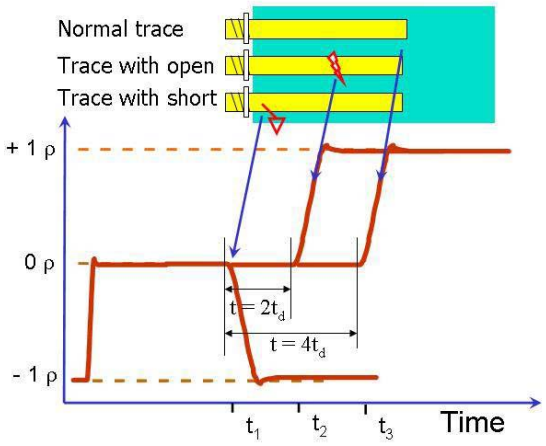


Figure 7: Schematic showing waveform difference for an open, short, and normal trace

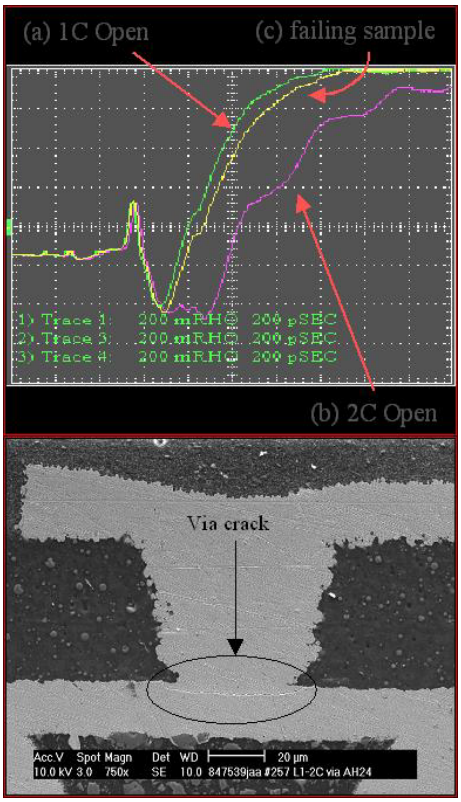


Figure 8: TDR waveform for the failing unit is open after 1C but before 2C. Cross-section reveals a micro via delamination between 2C and 1C.

Advanced Thermal Imaging Techniques and Applications

Thermal imaging is a non-destructive, non-invasive infrared (IR) technique. It detects the IR portion (~0.75um to 1000um) of the electromagnetic spectrum. Two wavelength bands from 2-5um and 7-14um are typically used. The IR system receives the IR radiation emitted from an object and converts it to electrical signals. These are then processed and displayed on a screen as a thermogram, either represented by IR intensity or absolute temperature [2, 3]. In the past, thermal imaging was often used in the semiconductor package industry to detect hotspots after applying current to the test structure.

Because of the increased pressure on thermal management for electronic packages to remove heat from the Si chip to ensure its reliable performance, thermal imaging techniques have been under development to detect Thermal Interface Material (TIM) defects in Integrated Heat Spreaders (IHS) in advanced microprocessors. Figure 9 shows the schematic stack-up of TIM sandwiched between the die and the IHS lid. There have been great demands to develop new TIMs, understand mechanisms of thermal failures, and determine heat distribution within packages for thermal model validation.

Conventional methods have their own pitfalls or limitations and do not always provide the complete, in-depth information needed to understand thermal failures. For example, an acoustic scan can provide information on physical defects but it is sometimes difficult to correlate with TIM thermal performance directly, because it is not a thermal response. With the advancement of hardware and software, thermal imaging offers great potential to address these challenges. Thermal imaging captures the surface temperature response of IHS as a function of time using a high-speed IR camera after powering up the die internally or applying pulsed external heating to the surface. The IR image is then analyzed using advanced image algorithms to reveal TIM defects or anomalies. With the presence of defects, the heat flow will be disrupted and that will be reflected on the surface thermal distribution [4, 5].

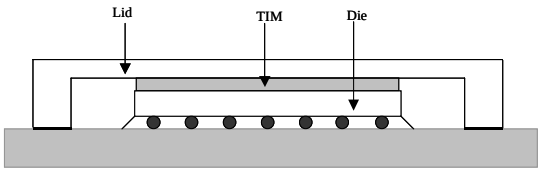


Figure 9: A schematic showing thin TIM is sandwiched between the die and the IHS lid

Figures 10a-c are the IHS thermal images of an assembly part at 15 millisecond (ms), 30ms, and 100ms after the die heater was powered up. It is obvious that the right side was hotter than the left side after power initiation (Figure 10a and 10b). In fact, there was a TIM thickness variation from left to right and the TIM at the left is thicker. However, this feature was not obvious from CSAM, as shown in Figure 10d. Note that the thermal contrast gradient between the good and the bad TIM region would gradually diminish if the IR image is captured at a later time frame, such as after 100ms (Figure 10c). This is a result of lateral heat diffusion. It should be noted that CSAM provides better spatial resolution on voiding defects, while this technique offers a direct linkage to thermal performance: the two techniques are therefore complementary.

Distinct failure patterns on defective TIM packages post reliability stress captured by thermal imaging are shown in Figure 11. Figure 11(a) was obtained by die power and Figure 11(b) by external flash. A consistent failure pattern was captured. The defective region is colder in the die power approach and becomes hotter in external flash; therefore, the color contrast is reversed. In contrast, the failure pattern was not obvious from the acoustic image in Figure 11c. By mapping out the defective region, this provides direction for further failure analysis, if desired. It is noted that a direct die power approach sometimes offers better sensitivity over external flashing. On the other hand, non-functional parts can be used for external flashing, which is advantageous for process development. Therefore, these two heating methods are complementary also.

It should be noted that thermal imaging has a broad range of applications. It can be used for detecting various types of sub-layer anomalies. One use of it is to analyze defects at bonded interfaces for 3-D integrated circuits after external pulsed flashing heating. Figure 12a shows an acoustic image of bonded wafers; bond interface voids can be seen at the center region of the wafer as marked by arrows in the blow up of the center region shown in Figure 12b. It is clearly seen that the voids appear as hotspots in the IR image in Figure 12c. Un-bonded areas (or regions of missing interconnections) appear as high intensity spots in the thermal image because they lead to non-uniform temperature distribution at the surface of the substrate when the sample is rapidly heated with a flash lamp.

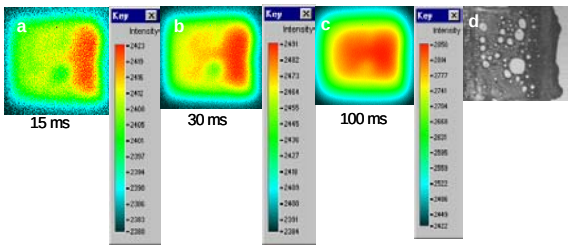


Figure 10: IHS thermal images of part with TIM thickness variation at a. 15 ms; b. 30 ms; c. 100 ms after the die heater was powered up; d. CSAM

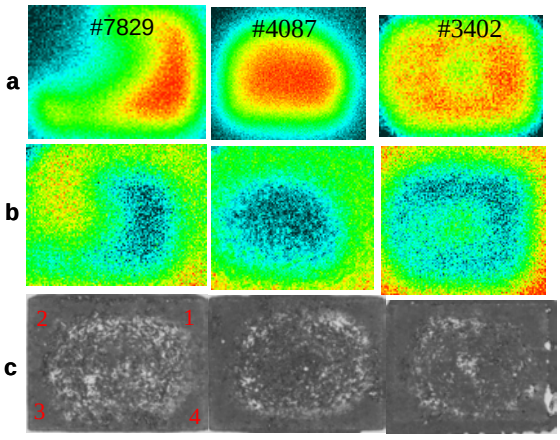


Figure 11: Three defective units post reliability stressing: a. IR images by die power; b. IR images using external flash; c. acoustic images

As expected, the smaller void disappears quickly as compared to the large void, when the temporal evolutions of the images are compared.

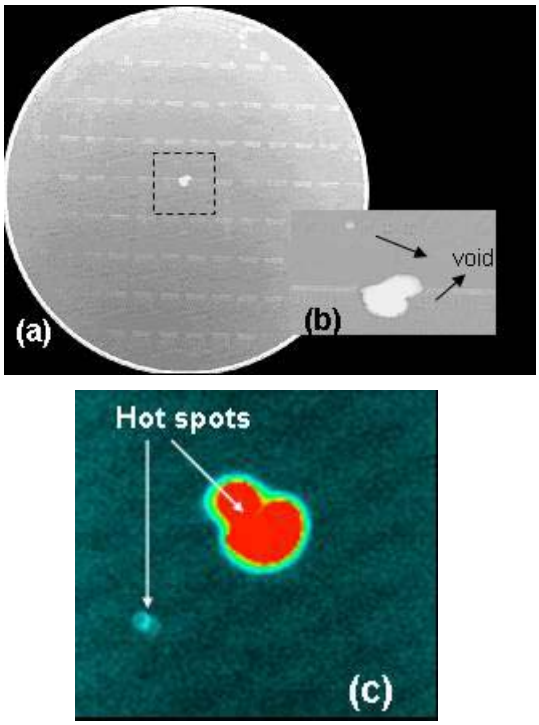


Figure 12: (a) CSAM image of a bonded wafer with voids at the center; (b) blow up of center region containing two voids; (c) thermal image of the same region containing the voids. The voids appear as hotspots in the thermal image.

Advanced thermal imaging techniques have the unique advantage of directly linking defects to package thermal performance by mapping out the defective region. These techniques can reveal defects that may be invisible to conventional approaches. It is critical to capture defect information at the very early stage by high-speed IR imaging in transient state, before significant lateral heat diffusion occurs. This is because the IR image of subsurface defects would appear blurred at the surface as a result of fast thermal diffusion as time elapses. Therefore, the resolution of defect and anomaly is strongly modulated by defect size and location. In addition to its benefit to thermal failure isolation, quantitative package thermal performance in transient state, upon development, can be determined by monitoring the temperature of the die through temperature sensors, and the IHS through IR imaging. Therefore, it has the potential to offer the advantage of thermal defects detection as well as thermal performance evaluation in one testing step. However, surface black coating is often required to enhance IR emission, which can limit its application scope.

Advanced Scanning Acoustic Microscopy

Acoustic, or more specifically, ultrasonic examination techniques offer the possibility of detecting and in many cases characterizing defects (cracks, voids, delaminations, etc.) in a non-invasive, fast, and reliable way. The development of high-tech devices, new techniques, and automation has made acoustic microscopy one of the most used fault-isolation techniques in the silicon industry. In this section we present some of the fundamentals of acoustic microscopy, discuss different techniques, and show specific applications linked to the microelectronic industry.

Scanning Acoustic Microscopy (SAM), also known as Acoustic Micro Imaging (AMI) uses high frequency ultrasonic waves to produce high-resolution images of a sample's interior structure. Unlike X-ray, visual inspection, and other Non-Destructive Testing (NDT) techniques, SAM makes use of the elastic properties of the materials to transmit the energy. Changes in the mechanical properties of the materials affect the propagation of the waves, and the effect associated with that interaction is used to generate images of specific sites within a sample [6].

Figure 13a shows the typical acoustic microscopy configuration in which water propagates the acoustic energy from a piezoelectric transducer to the specimen. The beam propagates through the material until it finds a discontinuity in its path (top surface, interconnecting layer, void, crack, etc.). If such a flaw (heterogeneity) is smaller than the cross-section of the sound beam, part of the beam bypasses the flaw and strikes the back wall. Each heterogeneity reflects an echo whose amplitude is proportional to the intensity of the returning wave. The transducer now acting as receiver transforms the mechanical oscillations in electrical signals, which are amplified and displayed in an oscilloscope. The reflections (back-wall and heterogeneity) are indicated according to their time of flight from the transmitter.

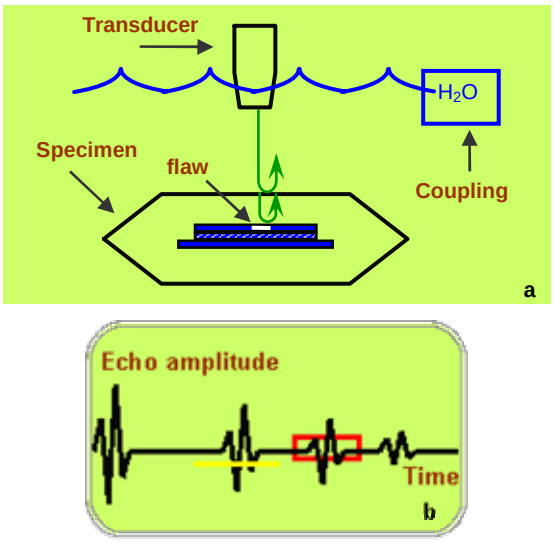


Figure 13: Acoustic microscopy operation principle schematic

The intensity of the reflected beam directly depends on the contrast between the acoustic impedances Z (Z=ρ(density)•c(wave speed)) at each interface. Acoustic impedance of air highly contrasts with that of any other material; therefore, the presence of a void in the path of the beam will reflect most of the energy of the perturbation. In addition, the size of the reflector, the frequency of the ultrasonic wave, material attenuation, the location of the reflector within the object, and the defect orientation will also determine the intensity of the reflection. Acoustic microscopy uses frequencies ranging from 5 to 400 MHz. In general the higher the scanning frequency, the higher the resolution of the images; however, increasing the frequency constrains the penetration depth of the beam.

The preceding description depicted the so called A-scan format, Figure 13b. There are other modes that utilize the amplitude and phase of the echoes to characterize the condition at the interfaces.

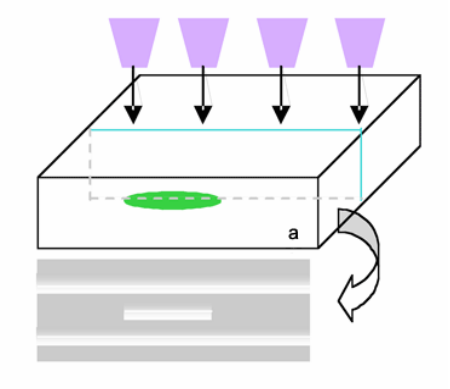


Figure 14: Schematics of a B-scan format

A series of A-scan data obtained along certain linear directions across the test object can be pieced together to form a B-scan, or in other words, cross-sectioning scan (Figure 14).

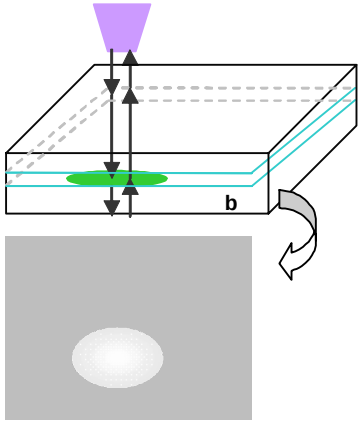


Figure 15: Schematics of a C-scan format

The C-scan presentation, also known as CSAM, Figure 15, provides a top view of the location and size of test specimen features. The plane of the image is parallel to the scan pattern of the transducer. In both formats, reflections from any discontinuity are recorded as dots whose brightness is modulated by the intensity of the reflections. Based on the nature of the acoustic ultrasonic technique, heterogeneities present in the path of the beam (specifically material interfaces, wires, solder material, voids, delamination, and cracks) will reflect part of the energy of the beam back giving rise to the generation of images. Some common examples are shown in Figures 16 and 17.

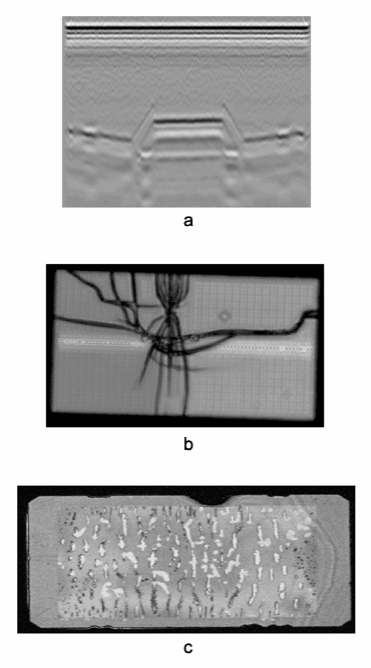


Figure 16: Examples of common packages defects, (a) tilt die, (b) die cracking, and (c) thermal lid sealing

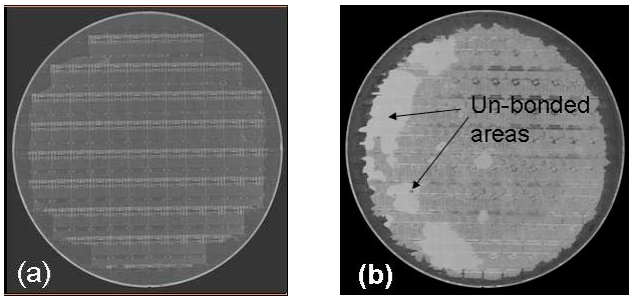


Figure 17: (a) CSAM of 300mm bonded wafers focusing at the bonded interface. The periodic contrast variation across the sample results from the integrated circuit metallization in every die; (b) CSAM of bonded wafer processed under non-optimal conditions. The bright regions correspond to voids or un-bonded regions at the bond interface. CSAM can successfully be used to identify such defects in advanced wafer-level package applications.

Laser Spallation Technique and Applications

Laser Spallation (LS) is an extremely high strain rate adhesion measurement technique of immense value in measuring the strength of interfaces in microelectronic components. In LS, since stress waves travel in the sample at material wave speeds, typical experimental strain rates are of the order of 10^5-$10^6 s^{-1}$. This is comparable with board-level strain rates in shock and drop tests and in contrast, strain rates in typical slow strain rate adhesion tests [7] such as 4-point bend or Cold Ball Pull (CBP) [8] are of the order of 10^{-5}-$10^0 s^{-1}$. One unique advantage of LS, therefore, is that it can be used to replicate failures that occur due to high impact or shock loads. A second advantage is that at high strain rates, low strain rate losses such as those due to plasticity or viscoelasticity are suppressed, resulting in strength values that are closer to the intrinsic strength of the interface. The basic premise of the laser spallation technique has been described in detail in earlier publications [9-12] and only an overview of the technique is presented here. In this paper we briefly discuss recent technical developments in the use of the LS tool. Specifically, three successful case studies are discussed.

Figure 18 provides a graphic description of the metrology. In LS, pulsed laser energy is incident on the sample on the ablation surface, which is the surface opposite to that with the interface of interest. Prior to the laser pulse, sample preparation involves coating the ablation surface with a metal layer, also referred to as an ablation layer, which typically is gold/palladium or aluminum. The ablation layer is then coated with a layer of waterglass (sodium silicate) that acts as a confining layer. When the pulsed YAG laser (wavelength of 1064nm) strikes the ablation layer, the metal heats up and tries to expand, but is prevented from expanding by the presence of the confining layer. This results in the generation of a mechanical compressive stress pulse that traverses through the substrate/film stack-up to reach the opposite surface, which will be referred to as the free surface. At the free surface the compressive stress pulse rebounds into a tensile stress pulse. If the magnitude of the tensile stress pulse is greater than the strength of the substrate/film interface, then spallation or debonding results.

Quantitatively, the displacement of the free surface when the compressive stress pulse impinges upon it is measured using a Michelson interferometer. Upon further reduction, this displacement data provide a magnitude of the impinging compressive stress pulse and subsequently, an estimate of the tensile stress that causes spallation.

The YAG laser in this experimental study has a pulse width of 3ns and so the entire process takes place over a time scale of the order of a few 100ns, resulting in the high strain rates with laser spallation. Yet another advantage with laser spallation is that it can be conveniently performed on test coupon-like samples and does not always require fully built packages. By performing experiments to quantitatively understand adhesion strength prior to expensive package builds and reliability stress exposure tests, LS offers a very convenient alternative as a quick-turn adhesion monitor.

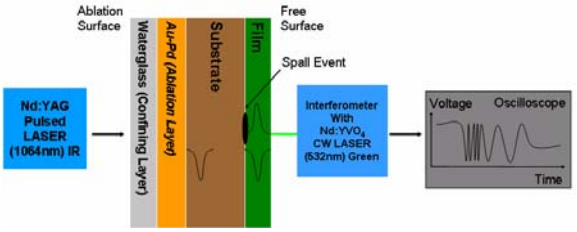


Figure 18: Graphic description of the laser spallation metrology. Substrate-film interface is the interface of interest.

Copper-to-dielectric (mostly epoxy-based) is an important interface in today's organic substrates. The quality of adhesion at this interface impacts the performance and reliability of a microelectronic package. The first successful quantitative application of the LS tool, an approach that utilizes the Michelson interferometer, was to estimate copper-dielectric adhesion strength in test coupons for organic substrates, see Figure 19. Five different dielectric types were examined, and the results of two of them are shown in Figure 19, labeled A and B. Dielectric type B was studied under ambient conditions as well as after exposure to 100 hours at 130°C and 85%RH. Adhesion strengths of the order of 10^2MPa were estimated, and a relative ranking of the flavors on the basis of strength as well as experimentally induced failure mode could be made. Significantly, ranking of the dielectric types was observed to be consistent with reliability performance. This successful study established the ability of LS to differentiate samples on the basis of their strength and failure modes.

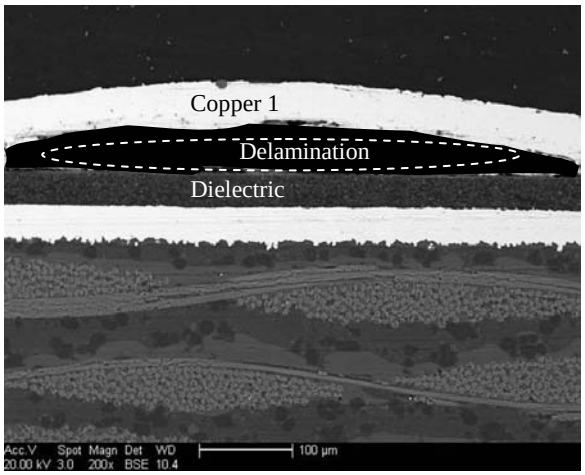
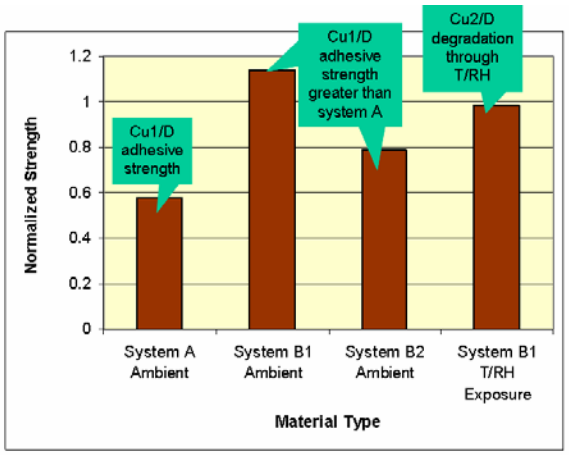


Figure 19(a): Copper-to-dielectric delamination, induced by laser spallation in system A



(b)

Figure 19 (b): Normalized strength estimates for different systems that indicate the ability of laser spallation to differentiate copper-dielectric samples on the basis of their strength and failure modes

The Electroless Nickel Immersion Gold (ENIG) plating process in Ball Grid Arrays (BGA) can lead to a solder joint fracture, which is a random and low ppm defect mode that occurs in the field due to mishandling or dropping of parts. LS, due to its very high strain rates, replicates stress conditions similar to drop or shock. Feasibility experiments on Pb as well as Pb-free BGA solders showed that the failure mode induced due to LS is the same as the solder joint fracture mode that is observed after CBP or drop test, i.e., at the intermetallic in the solder joint. Furthermore, the ability of LS to provide a quantitative strength estimate made it a valuable technique to select materials on the basis of their solder joint strength. Joint strengths measured using LS are of the order of ~300MPa or more. LS results were also consistent with the other techniques that were used to measure solder joint strength, i.e., CBP and shock tests.

In the above two studies, the estimate for adhesive strength was obtained directly from the experimental samples. In a substrate-film stack-up, if the surface of the film is not reflective, the Michelson interferometer cannot be directly utilized to obtain an estimate of the adhesion strength between the substrate and the film. A different approach is then required. This was established using a silicon-die attach test coupon where the film (die attach) surface is not reflective. In this approach, the critical laser ablation energy that causes silicon-die attach delamination is first established. Then, since the bare silicon substrate has a reflective surface, fringes are obtained from the surface of silicon at this critical energy using the Michelson interferometer. As a result, the shape and amplitude of the stress wave that eventually causes silicon-die attach delamination is well characterized. In

the final step, this stress pulse is input into a bi-layer finite element model of the silicon-die attach test coupon. Modeling results provide the entire stress history at the interface and thereby, the adhesion strength. For bare silicon, excellent agreement was obtained between the finite element model prediction and the experimental fringes, which validated this approach. For the bi-layer system, adhesion strength between silicon and die attach was measured to be ~300MPa. This methodology is a critical advancement of LS capabilities, since it expands the realm of tool application to systems that do not necessarily possess reflective films.

In addition to the above quantitative studies, semi-quantitative studies with silicon-die attach samples have also enabled ranking of material options. Factors such as the effect of moisture exposure, filler content in the die attach material, and silicon substrate roughness on silicon-die attach adhesion have also been well documented. Studies from the past have also established the value of LS towards die-level samples, particularly in ranking of low-K Inter Layer Dielectric (ILD) materials and the quality of Bump Limiting Metallurgy (BLM) interfaces. Due to its intrinsic nature, strength measurements from LS have the valuable potential to be used in accurate mechanics models. Recent developments have clearly shown the ability and application of LS to aid material selection as well.

3D X-Ray Computed Tomography for Electronic Packages Applications

3D X-ray CT was identified several years ago as a technique with fundamental feasibility to fill non-destructive fault isolation imaging gaps in next-generation microelectronic package technologies. In order to address this capability gap, the standard assembly imaging techniques of X-ray radiography/tomography needed to be extended into the next generation. Key technical drivers for 3D X-ray tomography are the need to non-destructively and quickly detect micron and sub-micron sized defects [13].

Figure 20 shows a typical X-ray CT configuration, in which the DUT is rotated in front of the X-ray source, while a detector collects X-ray images of the DUT at different tilt angles. The 2D images are computed to re-construct a true 3D model showing all internal features. By doing this, the analyst is able to perform virtual cross sectioning, planar grinding, and delayering, with the sample intact.

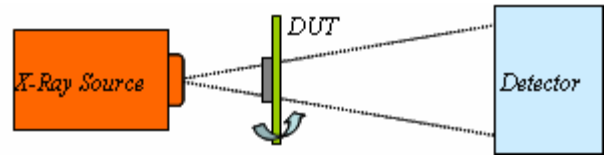


Figure 20: Typical X-ray computed tomography configuration

Package fail mechanisms such as C4 and BGA solder fatigue, Cu migration and trace cracking, microvoiding in C4, and BGA solder joints all present challenges to non-destructive imaging due to the small size of the defect (typically < 1 micron) and the complex geometries of the packages such as multi-layer stacks and materials resistant to X-ray penetration (for example thick Cu heat sinks, dense solders, and multi-layer interconnects).

Figure 21 shows a schematic of a multi-layer/multi-stacked die package while Figure 22 shows CT imaging of this package type. Figure 23 illustrates the capabilities of CT in resolving different planes and features of interest shown in Figure 22. As previously discussed, once a 3D CT model is complete, it can be manipulated to view any internal plane at any viewing angle. The same CT model can be used to view a selected area of interest from both grindback and cross-section perspectives. Package information such as multiple layers of interconnects, and multiple routing features can also be clearly illustrated using the CT technique.

Figure 23 illustrates a package's internal features including the C4 bump interconnect and the multiple layers of Cu routing and inter-layer connections (package via) and Plated Through Holes (PTH).

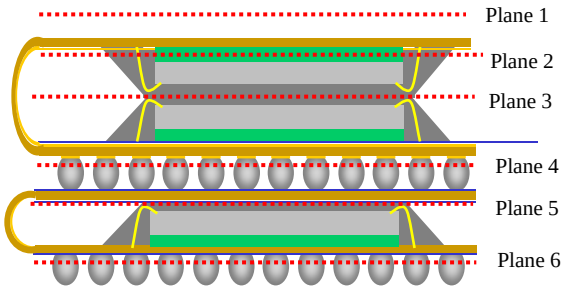


Figure 21: The images above show the view of various planes in the multi-layer/multi-die stacked package corresponding to the planes marked in Figure 22

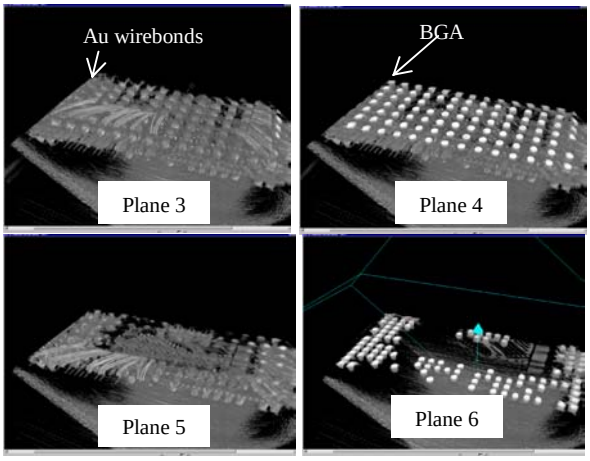


Figure 22: The images above show the view of various planes in the multi-layer/multi-die stacked package corresponding to the planes marked in Figure 21. The features of interest are also noted in these planes.

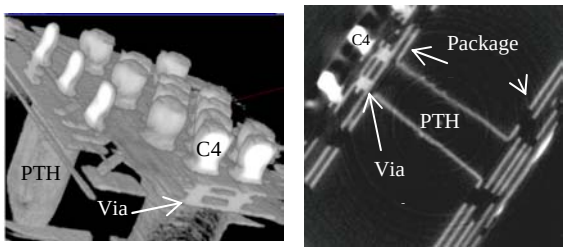


Figure 23: CT reconstruction illustrating a package's features including package via, PTH, and C4 bumps

Laser Deprocesing Techniques and Applications

Laser deprocessing, or as it's more commonly referred to, laser milling, is a non-contact, non-thermal, highly controlled and selective laser-based machining process. The tool that was used for the experiments that are reported in this section uses a high repetition rate, 10 to 60 Khz, and a 355Nm ultra-violet tripled YAG air-cooled laser from Coherent, the AVIA 355-3000. The overall design of the tool includes many features and options to allow the widest range of capabilities in materials processing, feature sizes, processing speeds, and flexibility. Spot sizes can be quickly changed to select between 8, 16, or 32 microns on the galvo side. On the fixed beam side, we currently have 5, 15, 25, 35, and 50 micron diameter spots. However, any size and shape spot can be created for the fixed beam application. Electronic package/die failure analysis requires a wide range of capabilities due to the varied nature of materials and designs used in the production of packages from the smallest over molded CSP to the largest next-generation CPU. That is why the tool is equipped with a scanning galvanometer for high-speed large-area processing, allowing beam scanning speeds of up to 960mm/sec. But when extreme precision is required, the tool is equipped with a fixed beam application where the beam/spot is fixed and the part is moved underneath the spot. The stages used to control and move the part have .1-micron steps and are repeatable. Moreover, the stages can be run at speeds of up to 350mm'sec. if required. Any shape or feature that can be programmed in CAD and output as a DXF can be imported and converted to a laser milling program. The laser tool can be programmed to control any number of about 12 different control variables allowing the most precise and repeatable laser recipes on the widest possible range of materials, designs, or requirements. Because of the range and number of laser variables, recipe development can be involved and time consuming. Part/material recipe libraries are critical to develop and maintain in order to speed the learning curve of new users and new requests [14, 15].

The key technical driver for laser deprocessing techniques is the continued reduction of package dimensions. Traditional manual sample deprocessing techniques are challenging when the package form factors are very small, because the possibility of damaging or missing defects is relatively high; this becomes a critical issue when only a few failing units are available for isolating defects and determining the root cause of the failure. Thus, laser deprocessing plays an important role in enabling fault isolation and failure analysis in those cases.

Laser milling with fully developed and refined recipes can make short work of selectively decapping mold compound to expose wirebonds for electrical testing or isolating the failure between package or die, which is shown in Figure 24. Further, laser programs can be employed to quickly and accurately cut the gold wires isolating the failure to selected entities, Figure 25.

Another application is the precise cutting of exposed copper traces of any width and thickness, Figure 26. The Soldermask is first easily and quickly removed at any location in any XY size or shape to expose the copper traces underneath, as can bee seen in Figure 27. The laser readily cuts the trace with a clean edge and minimal collateral damage.

Figure 24: Mold compound removed only at upper right side

(a) (b)

Figure 25: Optical images of (a) single wire laser cut, and (b) multiple wires cut. Time to process approximately 2 minutes.

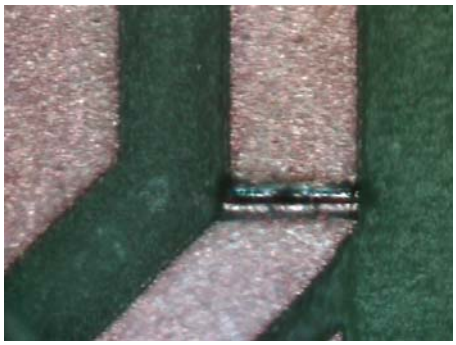


Figure 26: Trace width is approximately 28-microns wide

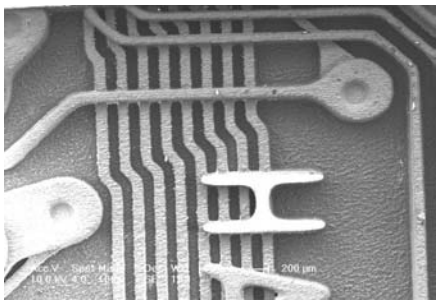


Figure 27: Soldermask and package dielectric laser ablated to expose two layers of substrate

ANALYTICAL TOOL CHALLENGES AND ROADMAP

There is an explosion in new package technology development to meet the increasing need for improved performance, integrated functions, reduced form factors, and reduced cost. Some of these package technologies include Wafer-Level Packaging (WLP) for MEMS, System in a Package (SiP), System on a Chip (SoP), stacked packages, etc. Traditional device and package technologies with shrinking geometries now have added complexities. For example, in stacked die packages, stacking eight to ten 50-micron-thick dies in a 1-mm thick package is possible. The interconnections between the die and the package could potentially be a combination of wirebond, flip chip, and through silicon vias on the dies. Silicon-package interaction issues will continue to be complex and critical for Failure Analysis with new technologies such as ultra low K dielectrics, 3D wafer stacking, electro-optical switching, and RF chips using SiGe.

Improvement and innovation in package analytical tools and techniques are necessary in advance of this new package technology being developed, in order to be effective in reducing the time-to information of potential fail mechanisms. In this section, we examine the challenges facing analytical tools associated with fault isolation, imaging, and Physical Failure Analysis (PFA).

Electrical fault isolation using current TDR capability or even the more recent 9psec rise time TDR systems have a limited resolution of 200um. This is far short of the 10um resolution capability required to identify the location of open failures in 10-12-layer organic substrates with embedded components, where line widths, spacing, and via dimensions will be around 10 microns.

Improvements in current non-destructive imaging are critical as component integration in packages increases and geometries shrink. One of the main challenges in imaging is resolving small defects or abnormalities not only spatially but, more importantly, in the axial direction. The ability to image a micron-sized defect non-destructively in a 10-die stacked package with multiple interconnects such as wirebond, flip chip, and BGA, and with a 12-layer substrate with embedded components and attached thermal solutions is indeed a challenge. Achieving this capability would significantly increase the FA success rate and reduce the time-to-information. Significant improvements in X-ray, acoustics, and magnetic imaging capability will be needed. In the area of X-ray imaging, several vendors are working to enhance the capability of 3D CT X-ray technology to demonstrate a 1um practical resolution on Intel packages. Non-destructive detection of a 1um interconnect separation in a

stacked die package, for example, would be one of the success criteria. In the area of acoustics, imaging multiple closely spaced interfaces such as in stacked die packages continues to be a major challenge to equipment vendors. At least three major vendors are working on improved and custom-designed transducers with improved resolution and die edge detection. The vendors are also developing software that can deconvolute the reflected acoustic signals to remove the effects of multiple reflections from die of equal thickness or spacings.

In the area of PFA, one of the biggest challenges is disassembly of multidie/multicomponent systems or packages without altering the defect or causing additional damage or artifacts. While current laser milling evaluations have shown promise, improvement in laser milling selectivity, end point detection, and minimization of laser damage needs to happen to make this package microsurgical capability useful. Another challenge in PFA is the ability to handle and test small fragile component parts after package disassembly. For example, handling and rebonding a 50-micron thin die removed from an 8-die stacked package or handling a small die or package fragment cut by the laser for surface analysis of a delaminated interface is very challenging.

In conclusion, the need to develop innovative and practical solutions to all of these challenges is imperative.

SUMMARY

We discussed how the accelerated development of package technologies has challenged the capabilities of traditional analytical tools and techniques to perform fault isolation and failure analysis. As a natural answer for such technical gaps, a continued effort to extend the capability of analytical tools and techniques has been required to enable Intel's fault isolation and failure analysis capabilities in new and next-generation package technologies. A detailed description of the operation principle of key advanced tools and techniques has been presented. In order to illustrate the usefulness of these analytical approaches, we reviewed some applications. Future challenges in next-generation package technologies, and the technical gaps in existing analytical capabilities, were discussed.

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